

App. Serial No. 10/561,625
Docket No.: NL 021505 US

BEST AVAILABLE COPY

Remarks

Claims 1-30 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated June 23, 2006 indicated an objection to the application title, an objection to claim 8 because of an informality and listed the following rejections: claim 1 and its dependents stand rejected under 35 U.S.C. § 112(1) regarding enablement; claims 19, 27 and their dependents stand rejected under 35 U.S.C. § 112(2) with regard to indefinite terminology; claim 18 stands rejected under 35 U.S.C. § 101; claims 1-9 and 11-30 stand rejected under 35 U.S.C. § 102(b) over Houston (U.S. 6,307,281); and claim 10 stands rejected under 35 U.S.C. § 103(a) over Houston in view of the Official Notice and further in view of Dinechin (U.S. 2003/0177482).

Regarding the objection to the application title, Applicant has provided a new title that is clearly indicative of the claimed invention and, as such, requests that the objection be removed.

Applicant respectfully traverses the Section 112(1) rejections of claims 1-18 because the specification does disclose both a processor coupled to the plurality of hardware resources and a processor comprising the plurality of hardware resources. For example, Fig. 2 shows a detailed view of CPU 14 of Fig. 1 and Fig. 1 shows CPU 14 coupled to a plurality of hardware resources of data processing system 10. Fig. 2 and the accompanying discussion illustrate but one example embodiment of the present invention. The specification elaborates in the discussion associated with Fig. 2 that while power control circuit 62 is shown as being used to control hardware resources disposed solely within CPU 14, the power control circuit can be used to control power dissipation of other hardware resources, including resources disposed elsewhere on the same integrated circuit and resources disposed on another integrated circuit (see, e.g., page 8, lines 11-17). CPU 14 is coupled via an internal bus 16 to a plurality of additional circuit components (see, e.g., Fig. 1 and page 5, lines 27-30). The additional circuit components have a variety of hardware resources, the power dissipation of which can be controlled by the power control circuit 62 of CPU 14 (see, e.g., page 8, lines 17-27). Accordingly, the Section 112(1) rejections of claims 1-18 are improper and Applicant requests that they be withdrawn.

App. Serial No. 10/561,625
Docket No.: NL 021505 US

BEST AVAILABLE COPY

Applicant traverses the Section 112(2) rejections of claims 19-30, because the claims are clearly understandable by one of ordinary skill in the art. Notwithstanding, in an effort to facilitate prosecution, Applicant has amended claims 19 and 27 to more particularly point out and distinctly claim the subject matter of the claimed invention. Specifically, the claims have been amended to clarify that the program code is executed on or by a processor that is coupled to a plurality of hardware resources. Applicant notes that the amendments are not being made to overcome any issues of patentability raised by the rejections in the Office Action. The claims are patently distinguishable over the cited references for the reasons discussed below, and are fully supported by the original disclosure. Therefore, Applicant requests that the Section 112(2) rejections be withdrawn.

Applicant traverses the Section 101 rejection of claim 18, because the medium is limited to tangible embodiments. Claim 18 is not directed towards intangible embodiments such as signals, carrier waves or waveforms as asserted by the Office Action. The claim is limited to a tangible signal-bearing medium through which a hardware definition program is transmitted or carried on. The transmission type media cited by the Office Action are limited to tangible embodiments such as the actual physical digital and analog communications links (see, e.g., page 9, line 30 to page 10, line 1). Notwithstanding, in an effort in facilitate prosecution, Applicant has amended claim 18 to clarify that it is limited to a signal-bearing tangible medium. As such, the Section 101 rejection of claim 18 is improper and Applicant requests that it be withdrawn.

Applicant traverses the Section 102(b) rejections of claims 1-9 and 11-30, because the cited portions of the Houston reference fail to correspond to all of the claimed limitations. Regarding independent claims 1, 19 and 27 (and as relevant to the claims that depend therefrom), the Office Action fails to cite any portion of the Houston reference that corresponds to claimed limitations directed to a processor coupled to a plurality of hardware resources. The Office Action cites to portions of the Houston reference that teach a processor 24 that includes elements 36 (see, e.g., Fig. 2 and col. 6, lines 56-67). The elements 36 are located on the processor 24, not coupled to the processor as in the claimed invention. Moreover, the Office Action fails to cite any portion of the Houston reference that corresponds to claimed limitations directed to selectively setting power modes of at least two of the plurality of hardware resources that

App. Serial No. 10/561,625
Docket No.: NL 021505 US

BEST AVAILABLE COPY

are coupled to the processor. The cited portion of the Houston reference only teaches that a processor 24 controls power dissipated by elements 36 that are located on the processor (see, e.g., Fig. 2, col. 6, lines 56-67), not selectively setting power modes of hardware resources that are coupled to the processor as in the claimed invention. Accordingly, the Section 102(b) rejections of claims 1, 19 and 27 are improper and Applicant requests that they be withdrawn.

The Section 102(b) rejections of dependent claims 2-9 and 11-18 which depend from claim 1, claims 20-26 which depend from claim 19, and claims 28-30 which depend from claim 27 are also improper for the reasons discussed above and Applicant requests that they be withdrawn. Moreover, the cited portions of the Houston reference fail to correspond to the claim 16 limitations directed to at least one hardware resource is disposed on a separate integrated circuit from the processor and the claim 17 limitations directed to an integrated circuit comprising the circuit arrangement of claim 1. The Office Action cites to the same part of the Houston reference (e.g., Fig. 2) for both rejections. Fig. 2 teaches a processor 24, a program memory 22 and a data memory 26. Assuming that the two memories are hardware resources, Fig. 2 can not teach that at least one hardware resource is disposed on a separate integrated circuit from the processor and an integrated circuit comprising the circuit arrangement of claim 1. Fig 2 either depicts an integrated circuit comprising elements 24, 22 and 26 or that memories 22 and 26 are disposed on a separate integrated circuit from processor 24.

Applicant traverses the Section 103(a) rejection of claim 10, because the cited portions of the Houston reference do not correspond to the claimed limitations as discussed above in connection with the Section 102(b) rejection of claim 1. In this regard, the rejection of claim 10 is improper because claim 10 depends from claim 1. The corresponding rejection thus relies upon the same (improper) rationale. Accordingly, Applicant requests that the Section 103(a) rejection of claim 10 be withdrawn.

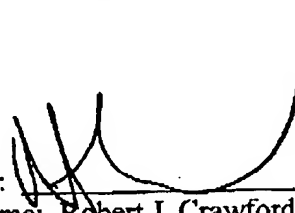
App. Serial No. 10/561,625
Docket No.: NL 021505 US

BEST AVAILABLE COPY

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of Philips Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
Philips Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

By: 
Name: Robert J. Crawford
Reg. No.: 32,122
(VLSI.491PA)

CUSTOMER NO. 24738